



N-Channel 40-V (D-S) MOSFET

CHARACTERISTICS

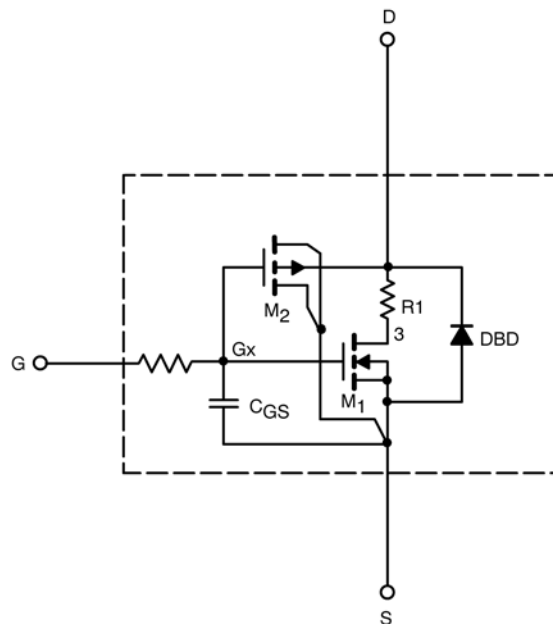
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.4		V
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	141		A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$	0.032	0.032	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$	0.042	0.041	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 5 \text{ A}$	11	15	S
Forward Voltage ^a	V_{SD}	$I_S = 1.7 \text{ A}$	0.72	0.79	V
Dynamic^b					
Input Capacitance	C_{iss}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	807	625	pF
Output Capacitance	C_{oss}		78	88	
Reverse Transfer Capacitance	C_{rss}		48	50	
Total Gate Charge	Q_g	$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$	13	14.4	nC
			6.4	6.6	
Gate-Source Charge	Q_{gs}	$V_{DS} = 20 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$	1.6	1.6	
Gate-Drain Charge	Q_{gd}		2.3	2.3	

Notes

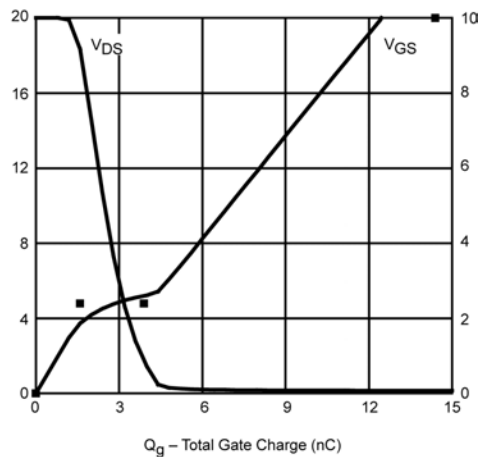
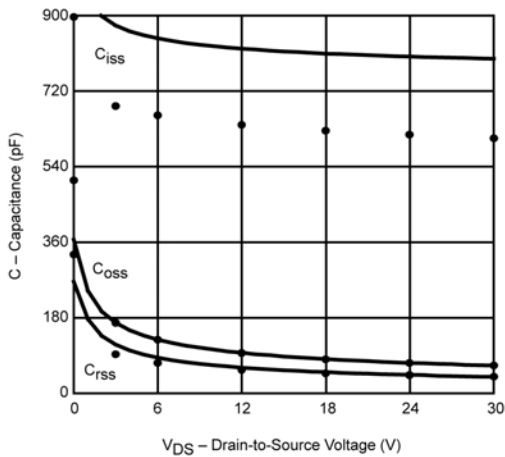
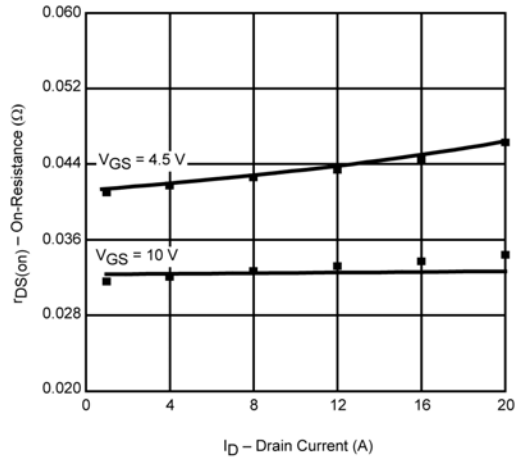
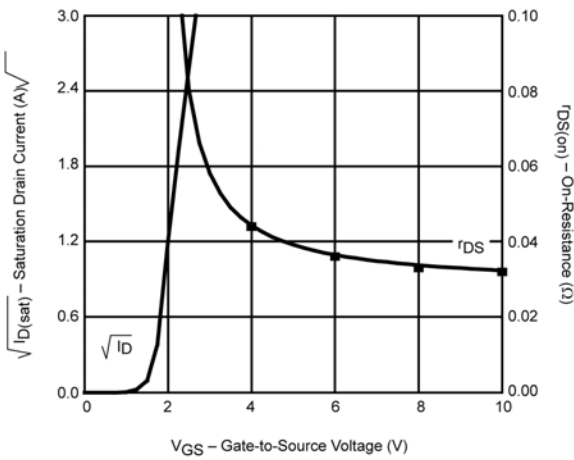
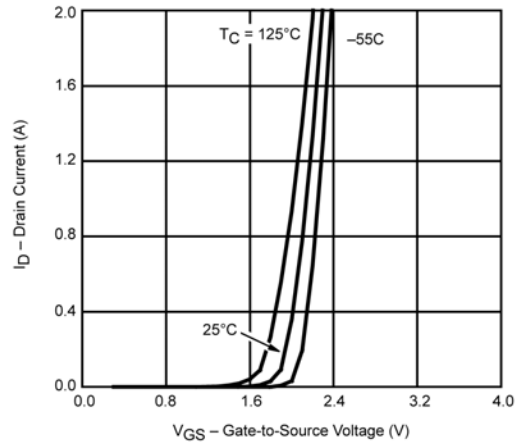
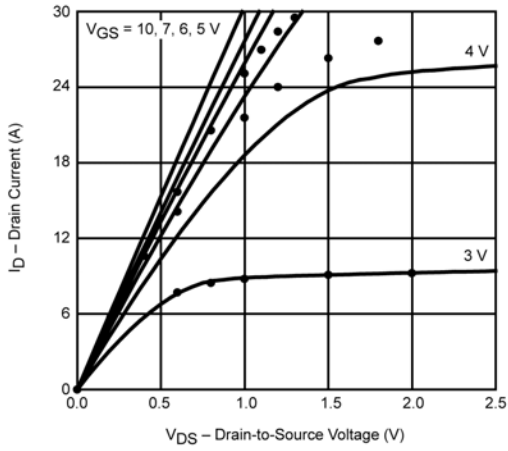
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.



SPICE Device Model Si4906DY

Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



Disclaimer

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